

TRIACs, 12A

Snubberless, Logic Level and Standard

FEATURES

- Medium current triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated TO-220AB package
- High commutation (4Q) or very high commutation (3Q) capability
- 12T series are **UL** certified (File ref: E320098)
- Packages are RoHS compliant

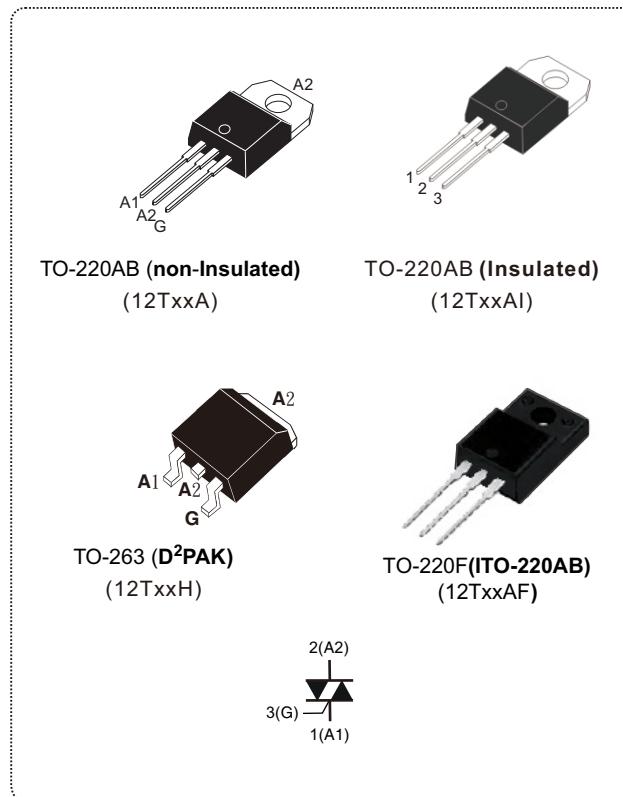
APPLICATIONS

ON/OFF or phase angle function in applications such as static relays, light dimmers and appliance motors speed controllers.

The snubberless versions (with suffix W) are especially recommended for use on inductive loads, because of their high commutation performances. The 12T series provides an insulated tab (rated at 2500V_{RMS}).

MAIN FEATURES

SYMBOL	VALUE	UNIT
I _{T(RMS)}	12	A
V _{DRM/V_{RRM}}	600 to 1000	V
I _{GT(Q1)}	5 to 50	mA



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNIT
RMS on-state current (full sine wave)	I _{T(RMS)}	TO-263/TO-220AB	12	A
Non repetitive surge peak on-state current (full cycle, T _j initial = 25°C)		TO-220AB insulated/TO-220F (ITO-220AB)		
I ² t Value for fusing	I ² t	F = 50 Hz	120	A
		F = 60 Hz		
Critical rate of rise of on-state current I _G = 2xI _{GT} , t _r ≤100ns	dI/dt	F = 100 Hz	50	A/μs
Peak gate current	I _{GM}	T _p = 20 μs	4	A
Average gate power dissipation	P _{G(AV)}	T _j = 125°C	1	W
Storage temperature range	T _{stg}		- 40 to + 150	°C
Operating junction temperature range	T _j		- 40 to + 125	

◎ ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise specified)

SNUBBERLESS and Logic level (3 quadrants)									
SYMBOL	TEST CONDITIONS	QUADRANT		12Txxxx				Unit	
				TW	SW	CW	BW		
$I_{GT}^{(1)}$	$V_D = 12\text{ V}$, $R_L = 30\Omega$	I - II - III	MAX.	05	10	35	50	mA	
V_{GT}		I - II - III	MAX.	1.3				V	
V_{GD}	$V_D = V_{DRM}$, $R_L = 3.3\text{K}\Omega$ $T_j = 125^\circ\text{C}$	I - II - III	MIN.	0.2				V	
$I_H^{(2)}$	$I_T = 100\text{ mA}$		MAX.	10	15	40	60	mA	
I_L	$I_G = 1.2 I_{GT}$	I - III	MAX.	10	20	50	70	mA	
		II		15	35	60	80		
$dV/dt^{(2)}$	$V_D = 67\% V_{DRM}$, gate open, $T_j = 125^\circ\text{C}$		MIN.	20	40	500	1000	V/ μs	
$(dI/dt)c^{(2)}$	$(dV/dt)c = 0.1\text{ V}/\mu\text{s}$ $T_j = 125^\circ\text{C}$		MIN.	3.5	6.5	-	-	A/ms	
	$(dV/dt)c = 10\text{ V}/\mu\text{s}$ $T_j = 125^\circ\text{C}$			1	2.9	-	-		
	Without snubber $T_j = 125^\circ\text{C}$			-	-	6.5	12		

◎ ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise specified)

Standard (4 quadrants)							
SYMBOL	TEST CONDITIONS	QUADRANT		12Txxxx			UNIT
				A	C	B	
$I_{GT}^{(1)}$	$V_D = 12\text{ V}$, $R_L = 30\Omega$	I - II - III	MAX.	10	25	50	mA
		IV		25	50	100	
V_{GT}		ALL		1.3			V
V_{GD}	$V_D = V_{DRM}$, $R_L = 3.3\text{K}\Omega$, $T_j = 125^\circ\text{C}$	ALL		0.2			V
$I_H^{(2)}$	$I_T = 500\text{ mA}$		MAX.	25	25	50	mA
I_L	$I_G = 1.2 I_{GT}$	I - III - IV	MAX.	30	40	50	mA
		II		40	80	80	
$dV/dt^{(2)}$	$V_D = 67\% V_{DRM}$, gate open, $T_j = 125^\circ\text{C}$		MIN.	100	200	400	V/ μs
$(dV/dt)c^{(2)}$	$(dI/dt)c = 5.3\text{ A/ms}$, $T_j = 125^\circ\text{C}$		MIN.	3	5	10	V/ μs

STATIC CHARACTERISTICS					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
$V_{TM}^{(2)}$	$I_{TM} = 17\text{ A}$, $t_P = 380\text{ }\mu\text{s}$	$T_j = 25^\circ\text{C}$	MAX.	1.55	V
$V_{t0}^{(2)}$	Threshold voltage	$T_j = 125^\circ\text{C}$	MAX.	0.85	V
$R_d^{(2)}$	Dynamic resistance	$T_j = 125^\circ\text{C}$	MAX.	35	$\text{m}\Omega$
I_{DRM} I_{RRM}	$V_D = V_{DRM}$ $V_R = V_{RRM}$	$T_j = 25^\circ\text{C}$	MAX.	5	μA
		$T_j = 125^\circ\text{C}$		1	mA

Note 1: Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: For both polarities of A2 referenced to A1.

THERMAL RESISTANCE					
SYMBOL				VALUE	UNIT
$R_{th(j-c)}$	Junction to case (AC)		TO-220AB, TO-263		1.4
			TO-220AB Insulated/TO-220F		2.3
$R_{th(j-a)}$	Junction to ambient	$S = 1 \text{ cm}^2$	TO-263		45
			TO-220AB Insulated, TO-220AB, TO-220F		60

S = Copper surface under tab.

PRODUCT SELECTOR						
PART NUMBER	VOLTAGE (xx)			SENSITIVITY	TYPE	PACKAGE
	600 V	800 V	1000 V			
12TxxA-B/12TxxAI-B	V	V	V	50 mA	Standard	TO-220AB
12TxxA-BW/12TxxAI-BW	V	V	V	50 mA	Snubberless	
12TxxA-C/12TxxAI-C	V	V	V	25 mA	Standard	
12TxxA-CW/12TxxAI-CW	V	V	V	35 mA	Snubberless	
12TxxA-SW/12TxxAI-SW	V	V	V	10 mA	Logic level	
12TxxA-TW/12TxxAI-TW	V	V	V	5 mA	Logic level	
12TxxH-B	V	V	V	50 mA	Standard	D ² PAK
12TxxH-C	V	V	V	25 mA	Standard	
12TxxH-SW	V	V	V	10 mA	Logic level	
12TxxH-CW	V	V	V	35 mA	Snubberless	
12TxxH-BW	V	V	V	50 mA	Snubberless	
12TxxH-TW	V	V	V	5 mA	Logic level	
12TxxAF-B	V	V	V	50 mA	Standard	TO-220F (ITO-220AB)
12TxxAF-C	V	V	V	25 mA	Standard	
12TxxAF-BW	V	V	V	50 mA	Snubberless	
12TxxAF-CW	V	V	V	35 mA	Snubberless	
12TxxAF-SW	V	V	V	10 mA	Logic level	
12TxxAF-TW	V	V	V	10 mA	Logic level	

AI: Insulated TO-220AB package

ORDERING INFORMATION					
ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
12TxxA-yy	12TxxA-yy	TO-220AB	2.0g	50	Tube
12TxxAI-yy	12TxxAI-yy	TO-220AB (insulated)	2.3g	50	Tube
12TxxAF-yy	12TxxAF-yy	TO-220F(ITO-220AB)	2.5g	50	Tube
12TxxH-yy	12TxxH-yy	TO-236(D ² PAK)	2.0g	50	Tube

Note: xx = voltage, yy = sensitivity

ORDERING INFORMATION SCHEME

	12	T	06	A - BW
Current				
12 = 12A				
Triac series				
Voltage				
06 = 600V				
08 = 800V				
10 = 1000V				
Package type				
A = TO-220AB (non-insulated)				
AI = TO-220AB (insulated)				
AF = TO-220F (ITO-220AB, insulated)				
H = TO-263 (D ² PAK)				
IGT Sensitivity				
B = 50mA Standard		BW = 50mA Snubberless		
C = 25mA Standard		CW = 35mA Snubberless		
SW = 10mA Logic Level		TW = 5mA Logic Level		

Fig.1 Maximum power dissipation versus RMS on-state current (full cycle)

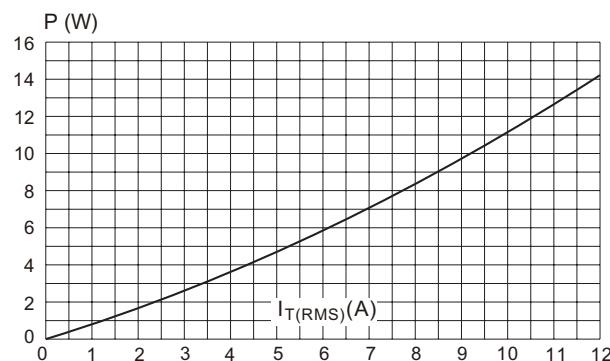


Fig.2 RMS on-state current versus case temperature (full cycle)

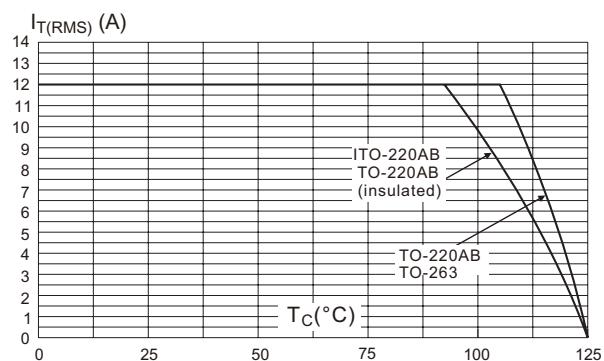


Fig.3 RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm)(full cycle)

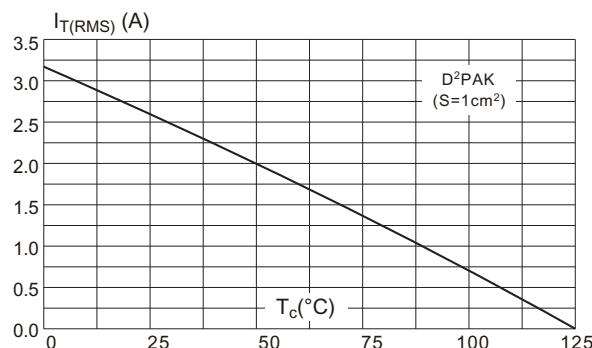


Fig.4 Relative variation of thermal impedance versus pulse duration.

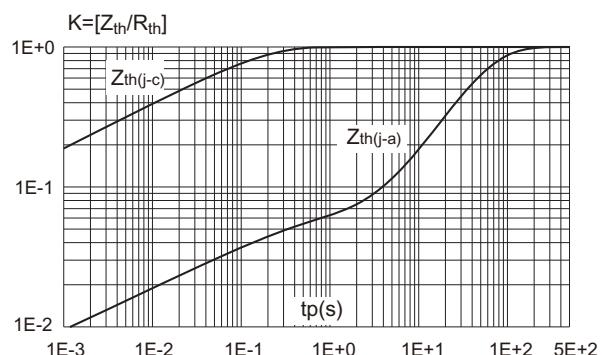


Fig.5 On-state characteristics (maximum values).

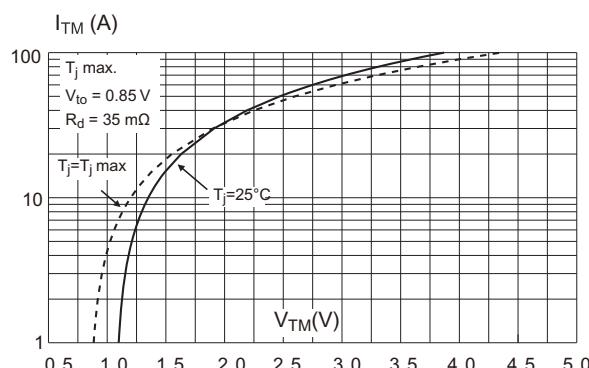


Fig.6 Surge peak on-state current versus number of cycles.

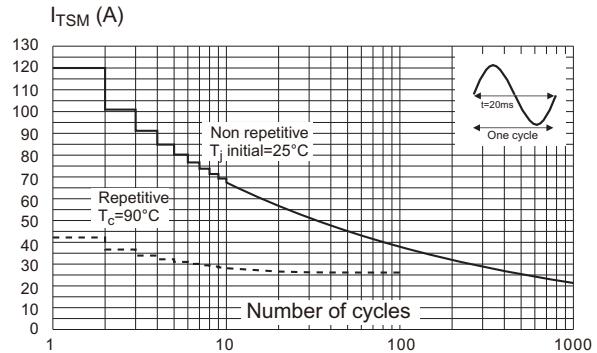


Fig.7 Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms. and corresponding value of I^2t .

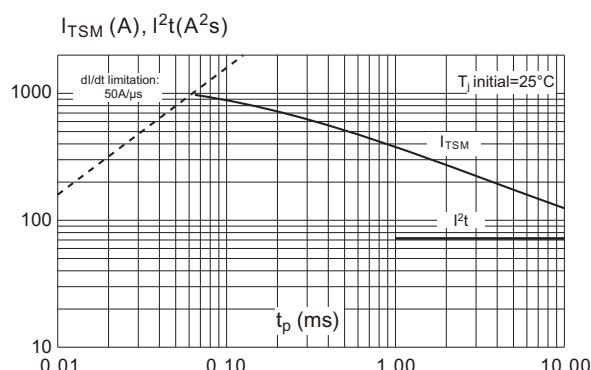


Fig.8 Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

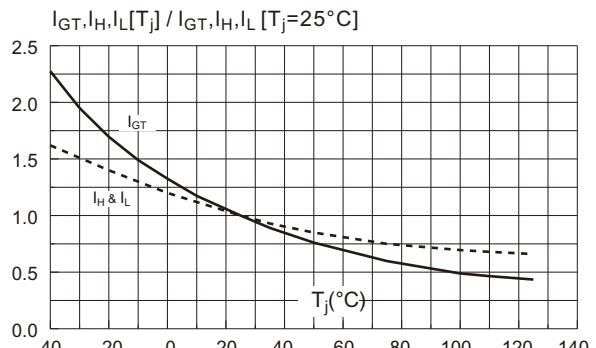


Fig.9 Relative variation of critical rate of decrease of main current versus $(dV/dt)c$ (typical values).

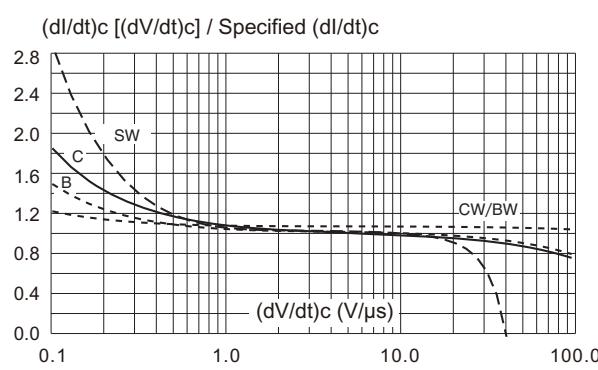


Fig.10 Relative variation of critical rate of decrease of main current versus $(dV/dt)c$ (typical values).

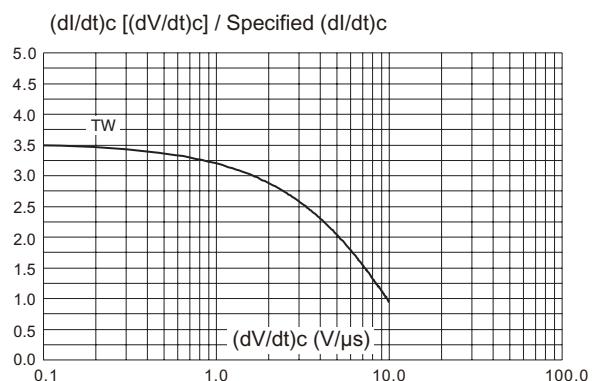


Fig.11 Relative variation of critical rate of decrease of main current versus junction temperature

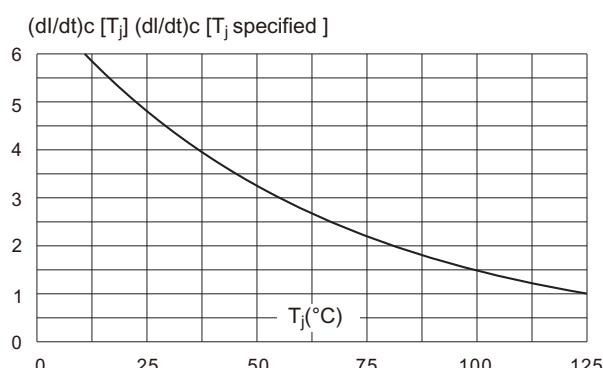
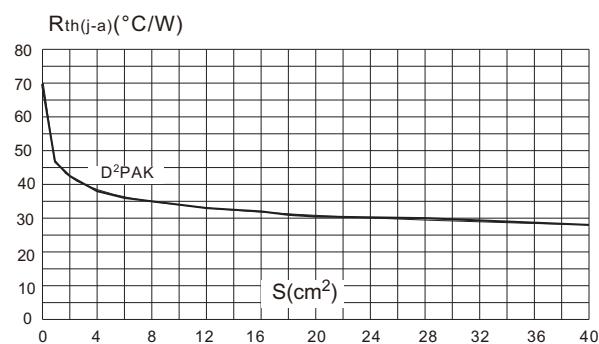
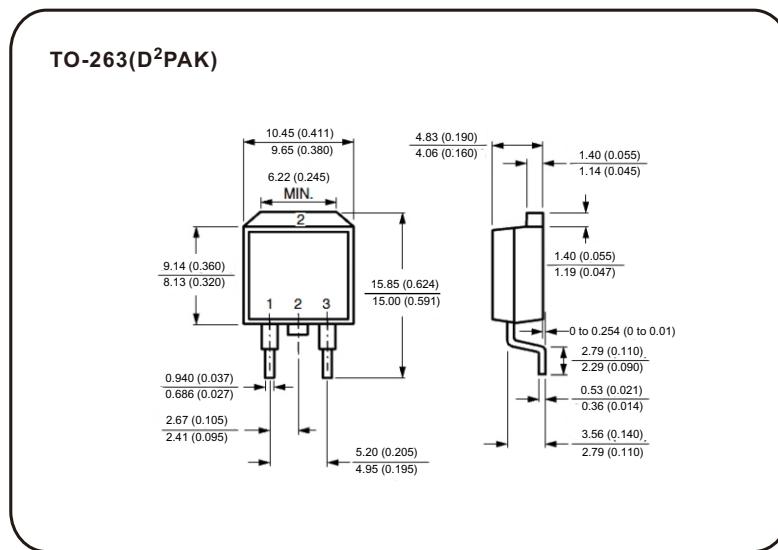
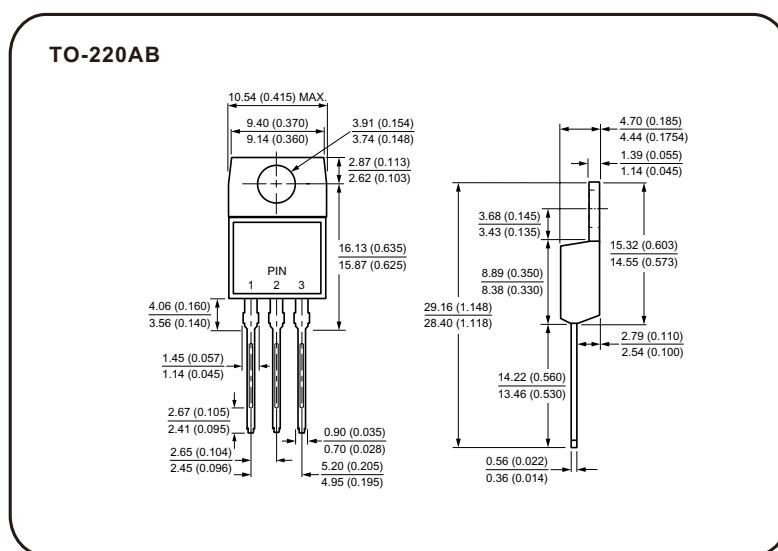


Fig.12 D²PAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35µm)



Case Style



All dimensions in millimeters(inches)

Case Style

